REMARKS

Claims 1-7 and 16-32 are pending in the present application. Claims 8-15 have been previously cancelled. No new claims are presented in this response.

The Examiner has rejected claims 1-7 & 23-27 under 35 U.S.C. 103(a) as being unpatentable over Lee, United States Patent No. 6,309,940, (hereafter "Lee") in view of Lai *et al*, United States Published Application No. 2002/0089017 (hereafter "Lai").

The Examiner has also rejected claims 16-22 & 28-32 under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Lai as applied to claims 1, 8 [sic, 7] & 23, and further in view of Tong *et al*, United States Patent No. 6,756,834 (hereafter "Tong").

Claim Rejections – 35 U.S.C. § 103

As previously noted claims 1-7 and 16-32 are all rejected under 35 U.S.C. § 103. Applicant addresses the rejection of these claims with respect to each set of claims.

Claim 1 *et seq.*

Examiner has rejected claims 1-7 as being obvious under 35 U.S.C. § 103 in view of Lee over Lai. However, Applicant finds the Examiner's citation of Lee and Lai to be deficient. Examiner claims the following:

> "Lee teaches an integrated circuit comprising: a silicon-controlled rectifier (column 1 lines 20-25); a first transistor (27, 28) of a first type (P-channel FET) integrally formed with the SCR including a first gate (37), a second transistor (25, 26) of a second type (N-channel FET) integrally formed with the SCR including a second gate (38); and a control circuit (V_{in}) which provides a first and second voltage to the first and second gates (37 & 38).

Applicant disagrees with Examiner's characterization in several regards:

First, it is unclear from the teachings of Lee whether the circuit constitutes a Silicon-Controlled Rectifier structure, especially a structure designed for ESD event protection. To be more specific, Examiner cites to lines 20-25 of Column 1 to support the position that Lee discloses an SCR. However, a careful review of the cited reference reveals that "Silicon Controlled Rectifier," or "SCR," is only mentioned once throughout the entire specification of Lee. Further, Lee admits describes a "related art semiconductor device," i.e. prior art device with respect to Lee, when describing Fig. 1 upon which the Examiner relies. Furthermore, there is no mention of SCR within the description of Fig. 1 in Lee, line 26 of Column 1 through line 41 of Column 2. The Examiner is respectfully requested to provide further support for the suitability of Lee for combination with Lai, especially considering the present invention's use as an Electronic Static Discharge protection device.

Additionally, the Examiner characterizes V_{IN} as a "control circuit" which provides a first and second voltage to the first and second gates (37 & 38). In reality, the device of Lee is nothing more than a CMOS Inverter. Thus, when V_{IN} is high, V_{OUT} is low; and when V_{OUT} is low, V_{IN} is high. Therefore, the gates of Lee do not disclose a SCR for ESD protection, but rather disclose an ordinary CMOS Inverter. In fact, this teachings of Lee appear to address the relatively low voltage required to trigger the CMOS device, in that "a voltage drop capable of turning on the bipolar transistors **36** and **35** occurs at a small critical current and the latch-up occurs in a case of the sufficiently high resistance between the N-well contact region **30** and the source region **28** of P channel FET or between the P-well contact region **29** and the source region **25** of N channel FET." As Applicant has previously noted, Lee attempts to "avoid latch-up with the presence of heavily dope region of buried layer formed at a predetermined portion in the wells." *See* Col. 2, ll. 45-47 (emphasis added). This has little, if any, relation to devices for

allowing a transient latch-up during an ESD event while preventing latch-up during ALL ordinary operation EXCEPT an ESD event, as generally desired by the present invention.

In summary, Lee is directly primarily toward avoiding low-voltage latch-up, not controlling the latch-up period associated with the large, transient voltages and currents of an ESD event. Furthermore, as already admitted by the Examiner, Lee clearly fails to disclose providing a first and second holding voltage. It is also easy to see that this limitation is not provided by Lai either when considering the practical combination of Lee and Lai. Specifically, with respect to the combination of Lee and Lai, Applicant believes the combination is deficient in several aspects, and therefore does not render the present invention obvious under 35 U.S.C. § 103.

First, it is important to note that Lai fails to teach a first and second FET with a first and second gate integrally formed in the SCR. In fact, none of the embodiments of Lai, including the embodiment described with respect to Figs. 7A and 7B, and cited by the Examiner, feature two FETs integrally formed in the device. Therefore, a person having ordinary skill in the art would allegedly have to rely on the teachings of Lee to provide a second FET integrally formed with the SCR. However, a review of the Lai references fails to teach a suitable modification that might be useful in providing the second integrated FET. Such an FET would require two P^+ doped regions separated by an N_{well}. However, there is no such location depicted in Fig. 7A for such an integrated FET. In fact, none of the embodiments depicted in Lai would allow for the modification or incorporation of a second FET. Furthermore, any modification necessary to provide such a suitable location would have a significant effect on the operation of the device as a whole. Therefore, it would take extensive experimentation and modifications to achieve the

configuration claimed by the present invention, far more than would be permitted to render the present invention obvious.

Second, as a second integrated FET is not provided in the configuration of Lai, it would be impossible to provide a control circuit attached to the first and second integrated FETs. Stepping through the necessary modifications of Lai to provide the present invention clearly suggests the present invention is non-obvious. After providing the second integrated FET by extensive modification and testing for suitability, it would then be necessary to provide a control circuit which would respond to a first voltage applied to the first and second gates to provide a first holding voltage, much less a second holding voltage. The brief statement cited by the Examiner in Lai is, at most, conclusory in that the circuit may be designed to control "the NMOS transistor to avoid latch-up while it is operated at the normal condition, but also control the additional PMOS transistor to let the ESD protection circuit to be much easily triggered." Indeed, this statement provides no basis for concluding that Lai, much less the combination of Lai and Lee, would provide a first and second holding voltage as claimed by the present invention.

Finally, it is not clear how the I/O pads nor the diode **108** of Lai would be incorporated into any combination of Lee and Lai. In fact, Lai depends heavily on the interaction of the I/O Pad in conjunction with the diode 108 to provide the functions described in Lai. The Examiner essentially omits these essential components of the alleged "control circuit" disclosed by Lai. Therefore, no reason exists to suggest that a person of ordinary skill in the art would inherently know how and where to incorporate the I/O pad and diode, if such an incorporation was at all possible. Instead, the Examiner's own failure to identify how these components interact with the alleged "control circuit" only reinforces the Applicant's argument for non-obviousness.

For all of the foregoing reasons, the combination of Lee and Lai is not believed to be render the present invention obvious. The Applicant respectfully requests reconsideration of the pending rejections directed toward claim 1, and all of its dependent claims, in view of the foregoing. Further, prompt allowance of the claims is respectfully requested.

Claim 16 *et seq.*

As with claim 1, the Applicant believes claim 16 to also be in condition for allowance in view of the Applicant's statements overcoming the obviousness rejection of Claim 1. Not considering for the moment Tong, Lee and Lai fail to teach an effective combination that would render claim 16 obvious. Specifically, the combination of Lee and Lai fail to teach a plurality of SCRs, each of the SCRs **including a p-type transistor and an n-type transistor integrally formed with the SCR.** Instead, as already noted, Lee and Lai disclose only a single integrated transistor. Therefore, Applicant believes claims 16 to be in condition for allowance. Therefore, dependent claims 17-22 are also in condition for allowance.

Claim 23 *et seq.*

As with claims 16-22, claims 23 are equally patentable in view of the comments made with respect to claim 1 and the non-obviousness of the present invention in view of Lee and Lai. As with claim 1, .

Moreover, Lee is even more inapplicable with respect to claim 23 and its dependent claims in view of the fact the claim requires an SCR having a holding voltage. As mentioned, the Examiner fails to properly identify how Lee teaches an SCR, other than simply citing to a single mention of the term in the entirety of the disclosure. Furthermore, the term holding

voltage is never mentioned in Lee either. Instead, the Examiner skips over the essential language "having a holding voltage." Therefore, the Examiner is respectfully requested to explain in detail, how the practical combination of Lee and Lai discloses all of the claimed limitations, including how Lee discloses an SCR, much less an SCR with a holding voltage. Absent such a detailed and supported disclosure of the Examiner's basis for the rejection, the Applicant is at a loss on how to fully and properly overcome the cited references.

Conclusion

Insofar as the Examiner's rejections were fully addressed, the present application is in condition for allowance. Issuance of a Notice of Allowability of all pending claims is therefore requested.

Respectfully submitted,

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